CLAIMS

We Claim:

1. An integrated circuit (IC) having programmable interconnections, the IC comprising:

configurable logic having a transmit variable-width port and a receive variable-width port;

a multi-gigabit transceiver having a transmit port and a receive port; and

a transmit variable-width interface coupling the transmit variable-width port of the configurable logic and the receive port of the multi-gigabit transceiver; and

a receive variable-width interface coupling the receive variable-width port of the configurable logic and the transmit port of the multi-gigabit transceiver.

2. The IC of Claim 1, wherein the variable-width ports of the configurable logic are configurable to widths of 1N, 2N, 4N and 8N, wherein N is an integer.

3. The IC of Claim 2, wherein the ports of the multi-gigabit transceiver have a width of 2N.

4. The IC of Claim 1, wherein the transmit variable-width interface comprises:

a first set of registers coupled to receive data values from the transmit variable width port of the configurable logic, wherein the first set of registers is clocked by a first clock signal; and

a set of multiplexers coupled to the first set of registers, wherein the set of multiplexers is coupled to the receive port of the multi-gigabit transceiver.

5. The IC of Claim 4, further comprising a second set of registers coupled to the set of multiplexers, wherein the second set of registers is clocked by a second clock signal.

6. The IC of Claim 5, wherein the rising edges of the slower of the first and second clock signals are aligned with falling edges of the faster of the first and second clock signals.

7. The IC of Claim 5, further comprising a delay flip-flop configured to delay the first clock signal by one half cycle of the second clock signal.

8. The IC of Claim 4, further comprising a transmit data width control circuit configured to generate enable signals for the first set of registers.

9. The IC of Claim 4, further comprising a transmit data width control circuit configured to generate control signals for the set of multiplexers.

10. The IC of Claim 4, wherein the first clock signal is selected in conjunction with a selected width of the transmit variable-width port.

11. The IC of Claim 1, wherein the transmit variable-width port and the receive variable-width port have different widths.

12. The IC of Claim 1, wherein the receive variable-width interface comprises:

a first set of registers coupled to receive data values from the transmit port of the multi-gigabit transceiver, wherein the first set of registers is clocked by a first clock signal; and

a second set of registers coupled to receive data values from the first set of registers and provide data values to the receive variable-width port of the configurable logic, wherein the second set of registers is clocked by a second clock signal.

13. The IC of Claim 12, further comprising a direct path between the transmit port of the multi-gigabit transceiver and a subset of the second set of registers.

14. A method of operating a device including configurable logic, configurable interconnections, a transceiver, and a variable-width interface circuit, the method comprising:

configuring the configurable logic to have a transmit port coupled to the variable-width interface circuit, wherein the transmit port is selected to have a first width that is selected from a plurality of widths;

routing data values having the first width from the configurable logic to the variable-width interface circuit on the transmit port in response to a first clock signal;

converting the data values having the first width to data values having a second width using the variable-width interface circuit; and

routing data values having the second width from the variable-width interface circuit to the transceiver in response to a second clock signal.

15. The method of Claim 14, further comprising selecting the first clock signal in conjunction with the selected first width, wherein the rising edges of the slower of the first and second clock signals are aligned with falling edges of the faster of the first and second clock signals.

16. The method of Claim 14, wherein the ratio of the first width to the second width is equal to the ratio of the frequency of the second clock signal to the frequency of the first clock signal.

17. The method of Claim 14, further comprising:

routing data values having the second width from the transceiver to the variable-width interface circuit in response to the second clock signal;

converting the data values received from the transceiver having the second width to data values having a third width, which is selected from a plurality of widths, using the variable-width interface circuit;

configuring the configurable logic to have a receive port coupled to the variable-width interface circuit, wherein the receive port is selected to have the third width; and

routing data values having the third width from the variable-width interface circuit to the configurable logic on the receive port in response to a third clock signal.

18. The method of Claim 17, wherein the first and third clock signals have the same frequency, and the first width is equal to the third width.